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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,938	02/05/2004	Chii-Ming Wu	TS03-493	6085

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EXAMINER	
WILSON, CHRISTIAN D	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,938	WU ET AL.	
	Examiner	Art Unit	
	Christian Wilson	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 04292004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: search history.

DETAILED ACTION

Claim Objections

1. Claim 19 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 10. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). For the purposes of examination, it will be assumed that claim 19 depends from claim 11.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 7, 9 – 11, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Wei *et al.*

Wei *et al.* (US 5,047,367) discloses a method of forming a metal silicide in a MOSFET device comprising the steps of providing a MOSFET device on a semiconductor substrate **10** with a conductive gate **21**, gate insulator **22**, and a heavily doped source **23**/drain **24** region, forming an interlayer material **11**, forming a metal layer **12**, performing an anneal procedure to

form a metal silicide **13** while forming a layer comprising the metal and interlayer material on insulator spacers **25**, and removing the layer from the insulator spacers [column 8, lines 1-5].

Regarding claim 7, Wei *et al.* further discloses a titanium interlayer material [column 5, lines 65-67].

Regarding claim 9, Wei *et al.* further discloses a nickel layer formed by physical vapor deposition [column 5, line 45; column 6, line 2] with a thickness of 50 – 300 Å [column 5, line 57].

Regarding claim 10, Wei *et al.* further discloses an RTA process performed at a temperature between 600 – 750 °C [column 6, lines 5-20].

Regarding claim 11, Wei *et al.* discloses a method of forming a metal silicide in a MOSFET device comprising the steps of providing a MOSFET device on a semiconductor substrate **10** with a conductive gate **21**, gate insulator **22**, and a heavily doped source **23**/drain **24** region, forming a titanium interlayer material **11**, forming a nickel layer **12**, performing an RTA procedure to form a metal silicide **13** while forming a layer comprising the Ni and Ti material on insulator spacers **25**, and removing the Ni-Ti layer from the insulator spacers [column 8, lines 1-5].

Regarding claim 18, Wei *et al.* further discloses a nickel layer formed by physical vapor deposition [column 5, line 45; column 6, line 2] with a thickness of 50 – 300 Å [column 5, line 57].

Regarding claim 19, Wei *et al.* further discloses an RTA process performed at a temperature between 600 – 750 °C [column 6, lines 5-20].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei *et al.* in view of Chu *et al.*

Wei *et al.* teaches a silicon dioxide gate oxide layer [column 7, line 35], but does not discuss thermal oxidation with a thickness of 10 – 100 Å. Chu *et al.* (6,767,831) teaches a thermal oxide with a thickness of 15 – 50 Å [column 3, lines 30-35]. It would have been obvious to one of ordinary skill in the art to use the thermal oxide of Chu *et al.* in the method of Wei *et al.* since this provides a deep submicron device with low parasitic current leakage.

6. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei *et al.* in view of Tsai *et al.*

Wei *et al.* teaches a polysilicon gate structure but does not discuss a particular gate thickness. Tsai *et al.* (US 5,702,972) teaches a polysilicon gate structure with a thickness of 2000 – 3000 Å [column 2, lines 49-50]. It would have been obvious to one of ordinary skill in the art to use the thicknesses of Tsai *et al.* in the method of Wei *et al.* since this provides a conventional thickness for etching gate structures.

7. Claims 4 – 6 and 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei *et al.* in view of Ishida *et al.*

Wei *et al.* teaches a silicon oxide spacer but does not discuss the width of the gate, the thickness of the spacer, or the depth of the source/drain regions. Ishida *et al.* (US 2003/0170969) teaches a MOSFET with a gate width of 0.25 μm and source/drain depth of 2000 Å [0003] and a spacer thickness of 200 – 1500 Å [0026]. It would have been obvious to one of ordinary skill in the art to use the device sizes of Ishida *et al.* in the method of Wei *et al.* since these provide high density and performance in ultra-large scale integrated devices.

8. Claims 8, 17, 20, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei *et al.* in view of Fang *et al.*

Wei *et al.* teaches the limitations of claims 7, 11, and 20 including a titanium layer, but does not discuss forming a 10 – 15 Å thick titanium layer by atomic layer deposition (ALD). Fang *et al.* (US 6,916,729) teaches a titanium layer with a thickness of 10 – 15 Å formed by ALD [column 5, lines 40-55]. It would have been obvious to one of ordinary skill in the art to use the ALD method of Fang *et al.* to form a thin Ti layer in the method of Wei *et al.* since this provides a preferable method of controlling deposition of a few atomic layers of titanium.

9. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wei *et al.* and Fang *et al.* as applied to claim 20 above, and further in view of Chu *et al.*

Wei *et al.* as modified by Fang *et al.* teaches a silicon dioxide gate oxide layer [column 7, line 35], but does not discuss thermal oxidation with a thickness of 10 – 100 Å. Chu *et al.* teaches a thermal oxide with a thickness of 15 – 50 Å [column 3, lines 30-35]. It would have been obvious to one of ordinary skill in the art to use the thermal oxide of Chu *et al.* in the method of Wei *et al.* since this provides a deep submicron device with low parasitic current leakage.

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wei *et al.* and Fang *et al.* as applied to claim 20 above, and further in view of Tsai *et al.*

Wei *et al.* as modified by Fang *et al.* teaches a polysilicon gate structure but does not discuss a particular gate thickness. Tsai *et al.* teaches a polysilicon gate structure with a thickness of 2000 – 3000 Å [column 2, lines 49-50]. It would have been obvious to one of ordinary skill in the art to use the thicknesses of Tsai *et al.* in the method of Wei *et al.* since this provides a conventional thickness for etching gate structures.

11. Claims 23 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei *et al.* and Fang *et al.* as applied to claim 20 above, and further in view of Ishida *et al.*

Wei *et al.* as modified by Fang *et al.* teaches a silicon oxide spacer but does not discuss the width of the gate, the thickness of the spacer, or the depth of the source/drain regions. Ishida *et al.* teaches a MOSFET with a gate width of 0.25 μm and source/drain depth of 2000 Å [0003] and a spacer thickness of 200 – 1500 Å [0026]. It would have been obvious to one of ordinary skill in the art to use the device sizes of Ishida *et al.* in the method of Wei *et al.* since these provide high density and performance in ultra-large scale integrated devices.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (571) 272-1886. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian Wilson, Ph.D.
Primary Examiner
Art Unit 2891

CDW